

Antonio González · Fernando Latorre
Grigorios Magklis

Processor Microarchitecture

An Implementation Perspective

Processor Microarchitecture An Implementation Perspective Fernando Latorre

Jin-Ying Zhang



Processor Microarchitecture An Implementation Perspective Fernando Latorre:

Processor Microarchitecture Antonio Gonzalez,Fernando Latorre,Grigorios Magklis,2010-03-03 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies

Processor Microarchitecture Antonio Gonzalez,Fernando Latorre,Grigorios Magklis,2022-05-31 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate

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General-Purpose Graphics Processor Architectures Tor M. Aamodt, Wilson Wai Lun Fung, Timothy G. Rogers, 2022-05-31 Originally developed to support video games graphics processor units GPUs are now increasingly used for general purpose non graphics applications ranging from machine learning to mining of cryptographic currencies GPUs can achieve improved performance and efficiency versus central processing units CPUs by dedicating a larger fraction of hardware resources to computation In addition their general purpose programmability makes contemporary GPUs appealing to software developers in comparison to domain specific accelerators This book provides an introduction to those interested in studying the architecture of GPUs that support general purpose computing It collects together information currently only found among a wide range of disparate sources The authors led development of the GPGPU Sim simulator widely used in academic research on GPU architectures The first chapter of this book describes the basic hardware structure of GPUs and provides a brief overview of their history Chapter 2 provides a summary of GPU programming models relevant to the rest of the book Chapter 3 explores the architecture of GPU compute cores Chapter 4 explores the architecture of the GPU memory system After describing the architecture of existing systems Chapters 3 and 4 provide an overview of related research Chapter 5 summarizes cross cutting research impacting both the compute core and memory system This book should provide a valuable resource for those wishing to understand the architecture of graphics processor units GPUs used for acceleration of general purpose applications and to those who want to obtain an introduction to the rapidly growing body of research exploring how to improve the architecture of these GPUs

Principles of Secure Processor Architecture Design Jakub Szefer, 2022-06-01 With growing interest in computer security and the protection of the code and data which execute on commodity computers the amount of hardware security features in today's processors has increased significantly over the recent years No longer of just academic interest security features inside processors have been embraced by industry as well with a number of commercial secure processor architectures available today This book aims to give readers insights into the principles behind the design of academic and commercial secure processor architectures Secure processor architecture research is concerned with exploring and designing hardware features inside computer processors features which can help protect confidentiality and integrity of the code and data executing on the processor Unlike traditional processor architecture research that focuses on performance efficiency and energy as the first order design objectives secure processor architecture design has security as the first order design objective while still keeping the others as important design aspects that need to be considered This book aims to present the different challenges of secure processor architecture design to graduate

students interested in research on architecture and hardware security and computer architects working in industry interested in adding security features to their designs It aims to educate readers about how the different challenges have been solved in the past and what are the best practices i e the principles for design of new secure processor architectures Based on the careful review of past work by many computer architects and security researchers readers also will come to know the five basic principles needed for secure processor architecture design The book also presents existing research challenges and potential new research directions Finally this book presents numerous design suggestions as well as discusses pitfalls and fallacies that designers should avoid

On-Chip Photonic Interconnects Christopher J. Nitta, Matthew Farrens, Venkatesh Akella, 2022-06-01 As the number of cores on a chip continues to climb architects will need to address both bandwidth and power consumption issues related to the interconnection network Electrical interconnects are not likely to scale well to a large number of processors for energy efficiency reasons and the problem is compounded by the fact that there is a fixed total power budget for a die dictated by the amount of heat that can be dissipated without special and expensive cooling and packaging techniques Thus there is a need to seek alternatives to electrical signaling for on chip interconnection applications Photonics which has a fundamentally different mechanism of signal propagation offers the potential to not only overcome the drawbacks of electrical signaling but also enable the architect to build energy efficient scalable systems The purpose of this book is to introduce computer architects to the possibilities and challenges of working with photons and designing on chip photonic interconnection networks

Datacenter Design and Management Benjamin C. Lee, 2022-05-31 An era of big data demands datacenters which house the computing infrastructure that translates raw data into valuable information This book defines datacenters broadly as large distributed systems that perform parallel computation for diverse users These systems exist in multiple forms private and public and are built at multiple scales Datacenter design and management is multifaceted requiring the simultaneous pursuit of multiple objectives Performance efficiency and fairness are first order design and management objectives which can each be viewed from several perspectives This book surveys datacenter research from a computer architect's perspective addressing challenges in applications design management server simulation and system simulation This perspective complements the rich bodies of work in datacenters as a warehouse scale system which study the implications for infrastructure that encloses computing equipment and in datacenters as distributed systems which employ abstract details in processor and memory subsystems This book is written for first or second year graduate students in computer architecture and may be helpful for those in computer systems The goal of this book is to prepare computer architects for datacenter oriented research by describing prevalent perspectives and the state of the art

Deep Learning Systems Andres Rodriguez, 2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by

state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to better collaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book

Quantum Computer Systems
Yongshan Ding, Frederic T. Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

Multithreading Architecture Mario

Nemirovsky, Dean Tullsen, 2022-05-31 Multithreaded architectures now appear across the entire range of computing devices from the highest performing general purpose devices to low end embedded processors Multithreading enables a processor core to more effectively utilize its computational resources as a stall in one thread need not cause execution resources to be idle This enables the computer architect to maximize performance within area constraints power constraints or energy constraints However the architectural options for the processor designer or architect looking to implement multithreading are quite extensive and varied as evidenced not only by the research literature but also by the variety of commercial implementations This book introduces the basic concepts of multithreading describes a number of models of multithreading and then develops the three classic models coarse grain fine grain and simultaneous multithreading in greater detail It describes a wide variety of architectural and software design tradeoffs as well as opportunities specific to multithreading architectures Finally it details a number of important commercial and academic hardware implementations of multithreading

Table of Contents Introduction Multithreaded Execution Models Coarse Grain Multithreading Fine Grain Multithreading Simultaneous Multithreading Managing Contention New Opportunities for Multithreaded Processors Experimentation and Metrics Implementations of Multithreaded Processors Conclusion *Space-Time Computing with Temporal Neural Networks* James E. Smith, 2022-05-31 Understanding and implementing the brain s computational paradigm is the one true grand challenge facing computer researchers Not only are the brain s computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain s computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain s neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing

study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described

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