CRCS SCHEME

USIN

15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019 Digital System Design using Verilog

Times: 3 have Mark. Marks: 80 Note: Answer any FIVE full questions, choosing

ONE full question from each module.

Mediale-1

- Explain with illustration, a simple design methodology followed
 - Explain the following constraints imposed in real world circuits
 - i) Noise margin iii) propagation delay. (RD Stanford) blank, that
 - Develop a verilog model for a 7-segment decoder, included in overrides the BCD i'p and causes all segments not to be life (85 Marks)

- 2 a Develop a version module of a debouncer for a puly button witch that unes a debounce 1996 Marriesa
 - interval of 10ms. Assume the system clock frequency is \$5 Mft.

 b. Design and develop a circuit and verifog reports a good to 10 counters. erstein, Williams Schools.
 - C. What is the distinction between a Moore and Meals thate state machine? 694 Marries

- Write a symbol for basic memory and explain its parts. 60th Minches
 - otto Marchest Explain about the multigent mem-
 - Compute the 12-bit ECC was a conceptable to the 8-bit data word "0110001". oba Markett

- Design a 64 K × 1000 component many using 16K × 8 bit component. 1000 Minches
- What is the difference as ween asynchronous static RAM and synchronous static RAM? otto Albertani
 - c. Using a Hamming Me, box many check hits are required for single error correction and
 - double enter detection to 4-bit data word? 4902 Marrison

Notice cliquities - No.

- Decay a preside incoder that has be inputs, \$0 : 15); a 4-bit encoded output, a[3:0] and a valid apput ic. "I" when any input is "I". Input i(0) has the highest pricety and i(15) is the
 - the concept of differential signaling. How does differential signaling improve noise CONTRACTOR STATE WHITE TARREST NAME.

OW

- What are the purpose of logic blocks and LO blocks in FPGA?
- Explain different types of PCB design.
 - Explain with a nest diagram of the internal organization of a CPLD.

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