Chapter 3 PROBLEMS

For all problems, use the device parameters provided in Chapter 3 (Tables 3.2 and 3.5) and the inside back book cover, unless otherwise mentioned. Also assume T = 300 K by default.

- [E,SPICE,3.2.2].
 - Consider the circuit of Figure 0.1. Using the simple model, with V_{Dec} = 0.7 V, solve for I_D.
 - b. Find I_D and F_D using the ideal diode equation. Use I_s = 10⁻¹⁴ A and T = 300 K.
 - e. Solve for F_{DE}, F_{DE}, and I_D using SPICE.
 - d. Repeat parts b and c using $I_3 = 10^{-16}$ A, T = 300K, and $I_3 = 10^{-14}$ A, T = 350 K.

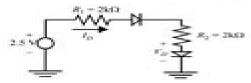


Figure 0.1 Resistor diode circuit.

- [M, None, 3.2.3] For the circuit in Figure 0.2, V_s = 3.3 V. Assume A_O = 12 μm², φ₀ = 0.65 V, and m = 0.5, N_d = 2.5 E16 and N_O = 5 E15.
 - a. Find In and Pre-
 - b. Is the diode forward- or reverse-biased?
 - e. Find the depletion region width, W., of the diode.
 - d. Use the parallel-plate model to find the junction capacitance, C_s
 - e. Set V_i = 1.5 V. Again using the parallel-plate model, explain qualitatively why C_j increases.

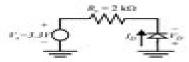


Figure 0.2 Series diode circuit

- 3. [E, None, 3.3.2] Figure 0.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current I_B for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: k_a^{*} = 115μA/V², V_B = 0.43 V, λ = 0.06 V⁻¹, PMOS: k_β^{*} = 30 μA/V², V_B = -0.4 V, λ = -0.1 V⁻¹. Assume (W.L) = 1.
 - a. NMOS: $F_{00} = 2.5 \text{ V}$, $F_{00} = 2.5 \text{ V}$. PMOS: $F_{00} = -0.5 \text{ V}$, $F_{D0} = -1.25 \text{ V}$.
 - b. NMOS: $V_{GS} = 3.3 \text{ V}$, $V_{DS} = 2.2 \text{ V}$. PMOS: $V_{GS} = -2.5 \text{ V}$, $V_{DS} = -1.8 \text{ V}$.
 - e. NMOS: $V_{CS} = 0.6 \text{ V}$, $V_{DS} = 0.1 \text{ V}$. PMOS: $V_{CS} = -2.5 \text{ V}$, $V_{DS} = -0.7 \text{ V}$.
- 4. [E, SPICE, 3.3.2] Using SPICE plot the I-V characteristics for the following devices.

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RS Peters

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