

CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019

Digital System Design using Verilog

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1. a. Explain with illustration, a simple design methodology followed in IC fabrication. (16 Marks)
 b. Explain the following constraints imposed in real world circuits:
 i) Noise margin ii) propagation delay. (10 Marks)
 c. Develop a verilog model for a 7-segment decoder, including an additional input, blank, that overrides the BCD input and causes all segments not to be lit. (14 Marks)

OR

2. a. Develop a verilog module of a debouncer for a push button switch that uses a debounced interval of 10ms. Assume the system clock frequency is 100 MHz. (16 Marks)
 b. Design and develop a circuit and verilog module for modulo-10 counters. (10 Marks)
 c. What is the distinction between a Moore and Mealy finite state machine? (14 Marks)

Module-2

3. a. Write a symbol for basic memory components and explain its parts. (16 Marks)
 b. Explain about the multiplexed memories. (10 Marks)
 c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". (14 Marks)

OR

4. a. Design a 64 K × 16-bit compressed memory using 16K × 8-bit component. (16 Marks)
 b. What is the difference between asynchronous static RAM and synchronous static RAM? (10 Marks)
 c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? (14 Marks)

Module-3

5. a. Design a priority decoder that has 16 inputs, $q[0:15]$; a 4-bit encoded output, $a[3:0]$ and a valid output is '1' when any input is '1'. Input $q[0]$ has the highest priority and $q[15]$ is the lowest priority. (16 Marks)
 b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? (14 Marks)

OR

6. a. What are the purpose of logic blocks and I/O blocks in FPGA? (16 Marks)
 b. Explain different types of PCB designs. (10 Marks)
 c. Explain with a neat diagram of the internal organization of a CPLD. (14 Marks)

1 of 2

Important Note: 1. De-compiling your answers, computerized data displayed over time on the remaining blank pages.
 2. Any revealing of identification, applied to evaluation and the questions written up, 42% to 50, will be treated as malpractice.

Sample Question Paper Electronics Schools9

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- Chapter 1: Introduction to Sample Question Paper Electronics Schools9
- Chapter 2: Essential Elements of Sample Question Paper Electronics Schools9
- Chapter 3: Sample Question Paper Electronics Schools9 in Everyday Life
- Chapter 4: Sample Question Paper Electronics Schools9 in Specific Contexts
- Chapter 5: Conclusion

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4. In chapter 3, the author will examine the practical applications of Sample Question Paper Electronics Schools9 in daily life. The third chapter will showcase real-world examples of how Sample Question Paper Electronics Schools9 can be effectively utilized in everyday scenarios.
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