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Antonio González · Fernando Latorre
Grigorios Magklis

Processor Microarchitecture

An Implementation Perspective

Springer

Processor Microarchitecture An Implementation Perspective Fernando Latorre

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Processor Microarchitecture Antonio Gonzalez,Fernando Latorre,Grigorios Magklis,2022-05-31 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies Processor Microarchitecture Antonio González,Fernando Latorre,Grigorios Magklis,2010-12-30 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate

students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies **General-Purpose Graphics Processor Architectures** Tor M. Aamodt,Wilson Wai Lun Fung,Timothy G. Rogers,2022-05-31 Originally developed to support video games graphics processor units GPUs are now increasingly used for general purpose non graphics applications ranging from machine learning to mining of cryptographic currencies GPUs can achieve improved performance and efficiency versus central processing units CPUs by dedicating a larger fraction of hardware resources to computation In addition their general purpose programmability makes contemporary GPUs appealing to software developers in comparison to domain specific accelerators This book provides an introduction to those interested in studying the architecture of GPUs that support general purpose computing It collects together information currently only found among a wide range of disparate sources The authors led development of the GPGPU Sim simulator widely used in academic research on GPU architectures The first chapter of this book describes the basic hardware structure of GPUs and provides a brief overview of their history Chapter 2 provides a summary of GPU programming models relevant to the rest of the book Chapter 3 explores the architecture of GPU compute cores Chapter 4 explores the architecture of the GPU memory system After describing the architecture of existing systems Chapters 3 and 4 provide an overview of related research Chapter 5 summarizes cross cutting research impacting both the compute core and memory system This book should provide a valuable resource for those wishing to understand the architecture of graphics processor units GPUs used for acceleration of general purpose applications and to those who want to obtain an introduction to the rapidly growing body of research exploring how to improve the architecture of these GPUs **Principles of Secure Processor Architecture Design** Jakub Szefer,2022-06-01 With growing interest in computer security and the protection of the code and data which execute on commodity computers the amount of hardware security features in today s processors has increased significantly over the recent years No longer of just academic interest security features inside processors have been embraced by industry as well with a number of commercial secure processor architectures available today This book aims to give readers insights into the principles behind the design of academic and commercial secure processor architectures Secure processor architecture research is concerned with exploring and designing hardware features inside computer processors features which can help protect confidentiality and integrity of the code and data executing on the processor Unlike traditional processor architecture research that focuses on performance efficiency and energy as the first order design objectives secure processor architecture design has security as the first order design objective while still keeping the others as important design aspects that need to be considered This book aims to present the different challenges of secure processor architecture design to graduate

students interested in research on architecture and hardware security and computer architects working in industry interested in adding security features to their designs It aims to educate readers about how the different challenges have been solved in the past and what are the best practices i e the principles for design of new secure processor architectures Based on the careful review of past work by many computer architects and security researchers readers also will come to know the five basic principles needed for secure processor architecture design The book also presents existing research challenges and potential new research directions Finally this book presents numerous design suggestions as well as discusses pitfalls and fallacies that designers should avoid **Datacenter Design and Management** Benjamin C. Lee,2022-05-31 An era of big data demands datacenters which house the computing infrastructure that translates raw data into valuable information This book defines datacenters broadly as large distributed systems that perform parallel computation for diverse users These systems exist in multiple forms private and public and are built at multiple scales Datacenter design and management is multifaceted requiring the simultaneous pursuit of multiple objectives Performance efficiency and fairness are first order design and management objectives which can each be viewed from several perspectives This book surveys datacenter research from a computer architect s perspective addressing challenges in applications design management server simulation and system simulation This perspective complements the rich bodies of work in datacenters as a warehouse scale system which study the implications for infrastructure that encloses computing equipment and in datacenters as distributed systems which employ abstract details in processor and memory subsystems This book is written for first or second year graduate students in computer architecture and may be helpful for those in computer systems The goal of this book is to prepare computer architects for datacenter oriented research by describing prevalent perspectives and the state of the art On-Chip Photonic Interconnects Christopher J. Nitta,Matthew Farrens,Venkatesh Akella,2022-06-01 As the number of cores on a chip continues to climb architects will need to address both bandwidth and power consumption issues related to the interconnection network Electrical interconnects are not likely to scale well to a large number of processors for energy efficiency reasons and the problem is compounded by the fact that there is a fixed total power budget for a die dictated by the amount of heat that can be dissipated without special and expensive cooling and packaging techniques Thus there is a need to seek alternatives to electrical signaling for on chip interconnection applications Photonics which has a fundamentally different mechanism of signal propagation offers the potential to not only overcome the drawbacks of electrical signaling but also enable the architect to build energy efficient scalable systems The purpose of this book is to introduce computer architects to the possibilities and challenges of working with photons and designing on chip photonic interconnection networks *Deep Learning Systems* Andres Rodriguez,2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute

consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to bettercollaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book Multithreading Architecture Mario Nemirovsky,Dean Tullsen,2022-05-31 Multithreaded architectures now appear across the entire range of computing devices from the highest performing general purpose devices to low end embedded processors Multithreading enables a processor core to more effectively utilize its computational resources as a stall in one thread need not cause execution resources to be idle This enables the computer architect to maximize performance within area constraints power constraints or energy constraints However the architectural options for the processor designer or architect looking to implement multithreading are quite extensive and varied as evidenced not only by the research literature but also by the variety of commercial implementations This book introduces the basic concepts of multithreading describes a number of models of multithreading and then develops the three classic models coarse grain fine grain and simultaneous multithreading in greater detail It describes a wide variety of architectural and software design tradeoffs as well as opportunities specific to

multithreading architectures Finally it details a number of important commercial and academic hardware implementations of multithreading Table of Contents Introduction Multithreaded Execution Models Coarse Grain Multithreading Fine Grain Multithreading Simultaneous Multithreading Managing Contention New Opportunities for Multithreaded Processors Experimentation and Metrics Implementations of Multithreaded Processors Conclusion Space-Time Computing with Temporal Neural Networks James E. Smith,2022-05-31 Understanding and implementing the brain s computational paradigm is the one true grand challenge facing computer researchers Not only are the brain s computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain s computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain s neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described **Quantum Computer Systems** Yongshan Ding,Frederic T. Chong,2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future

directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

Die-stacking Architecture Yuan Xie,Jishen Zhao,2022-05-31 The emerging three dimensional 3D chip architectures with their intrinsic capability of reducing the wire length promise attractive solutions to reduce the delay of interconnects in future microprocessors 3D memory stacking enables much higher memory bandwidth for future chip multiprocessor design mitigating the memory wall problem In addition heterogenous integration enabled by 3D technology can also result in innovative designs for future microprocessors This book first provides a brief introduction to this emerging technology and then presents a variety of approaches to designing future 3D microprocessor systems by leveraging the benefits of low latency high bandwidth and heterogeneous integration capability which are offered by 3D technology **Performance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU)** Hyesoon Kim,Richard Vuduc,Sara Baghsorkhi,Jee Choi,Wen-mei W. Hwu,2022-05-31 General purpose graphics processing units GPGPU have emerged as an important class of shared memory parallel processing architectures with widespread deployment in every computer class from high end supercomputers to embedded mobile platforms Relative to more traditional multicore systems of today GPGPUs have distinctly higher degrees of hardware multithreading hundreds of hardware thread contexts vs tens a return to wide vector units several tens vs 1 10 memory architectures that deliver higher peak memory bandwidth hundreds of gigabytes per second vs tens and smaller caches scratchpad memories less than 1 megabyte vs 1 10 megabytes In this book we provide a high level overview of current GPGPU architectures and programming models We review the principles that are used in previous shared memory parallel platforms focusing on recent results in both the theory and practice of parallel algorithms and suggest a connection to GPGPU platforms We aim to provide hints to architects about understanding algorithm aspect to GPGPU We also provide detailed performance analysis and guide optimizations from high level algorithms to low level instruction level optimizations As a case study we use n body particle simulations known as the fast multipole method FMM as an example We also briefly survey the state of the art in GPU performance analysis tools and techniques Table of Contents GPU Design Programming and Trends Performance Principles From Principles to Practice Analysis and Tuning Using Detailed Performance Analysis to Guide Optimization **Architectural and Operating System Support for Virtual Memory** Abhishek Bhattacharjee,Daniel Lustig,2022-05-31 This book provides computer engineers academic researchers new graduate students and seasoned practitioners an end to end overview of virtual memory We begin with a recap of foundational concepts and discuss not only state of the art virtual memory hardware and software support available today but also emerging research trends in this space The span of topics covers processor microarchitecture memory systems operating system design and memory allocation We show how efficient virtual memory implementations hinge on careful hardware and software cooperation and we discuss new research directions aimed at addressing emerging

problems in this space Virtual memory is a classic computer science abstraction and one of the pillars of the computing revolution It has long enabled hardware flexibility software portability and overall better security to name just a few of its powerful benefits Nearly all user level programs today take for granted that they will have been freed from the burden of physical memory management by the hardware the operating system device drivers and system libraries However despite its ubiquity in systems ranging from warehouse scale datacenters to embedded Internet of Things IoT devices the overheads of virtual memory are becoming a critical performance bottleneck today Virtual memory architectures designed for individual CPUs or even individual cores are in many cases struggling to scale up and scale out to today s systems which now increasingly include exotic hardware accelerators such as GPUs FPGAs or DSPs and emerging memory technologies such as non volatile memory and which run increasingly intensive workloads such as virtualized and or big data applications As such many of the fundamental abstractions and implementation approaches for virtual memory are being augmented extended or entirely rebuilt in order to ensure that virtual memory remains viable and performant in the years to come

Single-Instruction Multiple-Data Execution Christopher J. Hughes,2022-05-31 Having hit power limitations to even more aggressive out of order execution in processor cores many architects in the past decade have turned to single instruction multiple data SIMD execution to increase single threaded performance SIMD execution or having a single instruction drive execution of an identical operation on multiple data items was already well established as a technique to efficiently exploit data parallelism Furthermore support for it was already included in many commodity processors However in the past decade SIMD execution has seen a dramatic increase in the set of applications using it which has motivated big improvements in hardware support in mainstream microprocessors The easiest way to provide a big performance boost to SIMD hardware is to make it wider i e increase the number of data items hardware operates on simultaneously Indeed microprocessor vendors have done this However as we exploit more data parallelism in applications certain challenges can negatively impact performance In particular conditional execution non contiguous memory accesses and the presence of some dependences across data items are key roadblocks to achieving peak performance with SIMD execution This book first describes data parallelism and why it is so common in popular applications We then describe SIMD execution and explain where its performance and energy benefits come from compared to other techniques to exploit parallelism Finally we describe SIMD hardware support in current commodity microprocessors This includes both expected design tradeoffs as well as unexpected ones as we work to overcome challenges encountered when trying to map real software to SIMD execution

Power-Efficient Computer Architectures Magnus Själander,Margaret Martonosi,Stefanos Kaxiras,2022-05-31 As Moore s Law and Dennard scaling trends have slowed the challenges of building high performance computer architectures while maintaining acceptable power efficiency levels have heightened Over the past ten years architecture techniques for power efficiency have shifted from primarily focusing on module level efficiencies toward more holistic design styles based

on parallelism and heterogeneity This work highlights and synthesizes recent techniques and trends in power efficient computer architecture Table of Contents Introduction Voltage and Frequency Management Heterogeneity and Specialization Communication and Memory Systems Conclusions Bibliography Authors Biographies **Customizable Computing** Yu-Ting Chen,Jason Cong,Michael Gill,Glenn Reinman,Bingjun Xiao,2022-05-31 Since the end of Dennard scaling in the early 2000s improving the energy efficiency of computation has been the main concern of the research community and industry The large energy efficiency gap between general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their impact on performance and energy efficiency We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful reference basis for further research design and implementation for large scale deployment in future computing systems *Automatic Parallelization* Samuel Midkiff,2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading **Data Orchestration in Deep Learning Accelerators** Tushar Krishna,Hyoukjun Kwon,Angshuman Parashar,Michael Pellauer,Ananda Samajdar,2022-05-31 This Synthesis Lecture focuses on techniques for efficient data orchestration within DNN accelerators The End of Moore s Law coupled with the increasing growth in deep learning and other AI applications has led to the emergence of custom Deep Neural Network DNN accelerators for energy efficient inference on edge devices Modern DNNs have millions of hyper parameters and involve billions of computations this necessitates extensive data movement from

memory to on chip processing engines It is well known that the cost of data movement today surpasses the cost of the actual computation therefore DNN accelerators require careful orchestration of data across on chip compute network and memory elements to minimize the number of accesses to external DRAM The book covers DNN dataflows data reuse buffer hierarchies networks on chip and automated design space exploration It concludes with data orchestration challenges with compressed and sparse DNNs and future trends The target audience is students engineers and researchers interested in designing high performance and low energy accelerators for DNN inference Deep Learning for Computer Architects Brandon Reagen,Robert Adolf,Paul Whatmough,Gu-Yeon Wei,David Brooks,2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context **A Primer on Hardware Prefetching** Babak Falsafi,Thomas F. Wenisch,2022-06-01 Since the 1970 s microprocessor based digital platforms have been riding Moore s law allowing for doubling of density for the same area roughly every two years However whereas microprocessor fabrication has focused on increasing instruction execution rate memory fabrication technologies have focused primarily on an increase in capacity with negligible increase in speed This divergent trend in performance between the processors and memory has led to a phenomenon referred to as the Memory Wall To overcome the memory wall designers have resorted to a hierarchy of cache memory levels which rely on the principal of memory access locality to reduce the observed memory access time and the performance gap between processors and memory Unfortunately important workload classes exhibit adverse memory access patterns that baffle the simple policies built into modern cache hierarchies to move instructions and data across cache levels As such processors often spend much time idling upon a demand fetch of memory blocks that miss in higher cache levels

Prefetching predicting future memory accesses and issuing requests for the corresponding memory blocks in advance of explicit accesses is an effective approach to hide memory access latency There have been a myriad of proposed prefetching techniques and nearly every modern processor includes some hardware prefetching mechanisms targeting simple and regular memory access patterns This primer offers an overview of the various classes of hardware prefetchers for instructions and data proposed in the research literature and presents examples of techniques incorporated into modern microprocessors

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