

Government Girls' Polytechnic, Bilaspur

Name of the Lab: Digital Electronics Lab

Practical: Digital Electronics Lab

Class: 3rd Semester (ET&T), 3rd Semester (CS) FOR ET&T

Teachers Assessment: 10 End Semester Examination: 50 FOR CS

Teachers Assessment: 20 End Semester Examination: 50

EXPERIMENT No- 1

OBJECTIVE; - Verify Truth Table of Logic Gates (AND, OR, NOT, NAND & NOR Gates).

EQUIPMENT REQUIRED: - All the basic gate mention in the fig.

THEORY: There are different gates available in digital electronic filed. Which is used to perform the different tasks they are as follow-

AND GATE: - This gate is used for the multiplication of two binary digits.

OR GATE: - This gate is used for the addition of two binary digits.

NOT GATE: - This gate gives the compliment of given binary digit.

NAND GATE: - This gate is used for giving compliment of multiplication of two binary digits.

NOR GATE: - This gate is used for giving compliment of the addition of two binary digits

DAIGRAMS:-

2-Input AND gate



70	B	Chartpaut
0	C)	0
0	1	0
1.	0	0
1	1	1

1-input NOT gate

2-input OR gate



10	13	Output
O	0	0
O	1	1
1	0	1
1	1.	1.

2-input NAND gate

Polytechnic Electronics Lab Manual

Jessica J Manson

Polytechnic Electronics Lab Manual:

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