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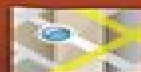
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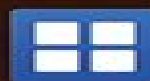
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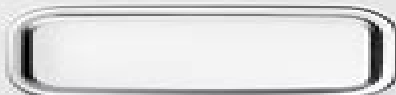
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# Samsung Galaxy Y Duos S61user Guide

**Katrin Zwirglmaier**



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web the i 2 c master is byte oriented and interrupt based the number of interrupts generated is kept at a minimum by automatic handling of most incidents the software driver complexity and code size are reduced by auto triggering of operations and a special smart mode which can be enabled by the smart mode enable bit in the control b register

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web c bus is a two wire serial bus with multiple possible masters and multiple possible slaves connected to each other through two wires the two wires consists of a clock line scl and a data line sda with both lines being bi directional

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub modules spi serial peripheral interface i2c inter integrated circuit the inter integrated circuit commonly referred to as i2c is a synchronous two wire bidirectional serial communications bus

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