

CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019

Digital System Design using Verilog

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1. a. Explain with illustration, a simple design methodology followed in IC fabrication. (16 Marks)
 b. Explain the following constraints imposed in real world circuits:
 i) Noise margin ii) propagation delay. (10 Marks)
 c. Develop a verilog model for a 7-segment decoder, including an additional input, blank, that overrides the BCD input and causes all segments not to be lit. (14 Marks)

OR

2. a. Develop a verilog module of a debouncer for a push button switch that uses a debounced interval of 10ms. Assume the system clock frequency is 100 MHz. (16 Marks)
 b. Design and develop a circuit and verilog module for modulo-10 counters. (10 Marks)
 c. What is the distinction between a Moore and Mealy finite state machine? (14 Marks)

Module-2

3. a. Write a symbol for basic memory components and explain its parts. (16 Marks)
 b. Explain about the multiplex memories. (10 Marks)
 c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". (14 Marks)

OR

4. a. Design a 64 K \times 16-bit computer memory using 16K \times 8 bit component. (16 Marks)
 b. What is the difference between asynchronous static RAM and synchronous static RAM? (10 Marks)
 c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? (14 Marks)

Module-3

5. a. Design a priority decoder that has 16 inputs, $q[0:15]$; a 4-bit encoded output, $a[3:0]$ and a valid output is '1' when any input is '1'. Input $q[0]$ has the highest priority and $q[15]$ is the lowest priority. (16 Marks)
 b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? (14 Marks)

OR

6. a. What are the purpose of logic blocks and I/O blocks in FPGA? (16 Marks)
 b. Explain different types of PCB designs. (10 Marks)
 c. Explain with a neat diagram of the internal organization of a CPLD. (14 Marks)

1 of 2

Important Note: 1. De-compiling your answers, computerized data displayed over time on the remaining blank pages.
 2. Any revealing of identification, applied to evaluation and, the questions written up, 42% to 50, will be treated as malpractice.

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Sabine Zange



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Table of Contents Sample Question Paper Electronics Schools9

1. Understanding the eBook Sample Question Paper Electronics Schools9
 - The Rise of Digital Reading Sample Question Paper Electronics Schools9
 - Advantages of eBooks Over Traditional Books
2. Identifying Sample Question Paper Electronics Schools9
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Sample Question Paper Electronics Schools9
 - User-Friendly Interface
4. Exploring eBook Recommendations from Sample Question Paper Electronics Schools9
 - Personalized Recommendations
 - Sample Question Paper Electronics Schools9 User Reviews and Ratings
 - Sample Question Paper Electronics Schools9 and Bestseller Lists

5. Accessing Sample Question Paper Electronics Schools9 Free and Paid eBooks
 - Sample Question Paper Electronics Schools9 Public Domain eBooks
 - Sample Question Paper Electronics Schools9 eBook Subscription Services
 - Sample Question Paper Electronics Schools9 Budget-Friendly Options
6. Navigating Sample Question Paper Electronics Schools9 eBook Formats
 - ePub, PDF, MOBI, and More
 - Sample Question Paper Electronics Schools9 Compatibility with Devices
 - Sample Question Paper Electronics Schools9 Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Sample Question Paper Electronics Schools9
 - Highlighting and Note-Taking Sample Question Paper Electronics Schools9
 - Interactive Elements Sample Question Paper Electronics Schools9
8. Staying Engaged with Sample Question Paper Electronics Schools9
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Sample Question Paper Electronics Schools9
9. Balancing eBooks and Physical Books Sample Question Paper Electronics Schools9
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Sample Question Paper Electronics Schools9
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Sample Question Paper Electronics Schools9
 - Setting Reading Goals Sample Question Paper Electronics Schools9
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Sample Question Paper Electronics Schools9
 - Fact-Checking eBook Content of Sample Question Paper Electronics Schools9
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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