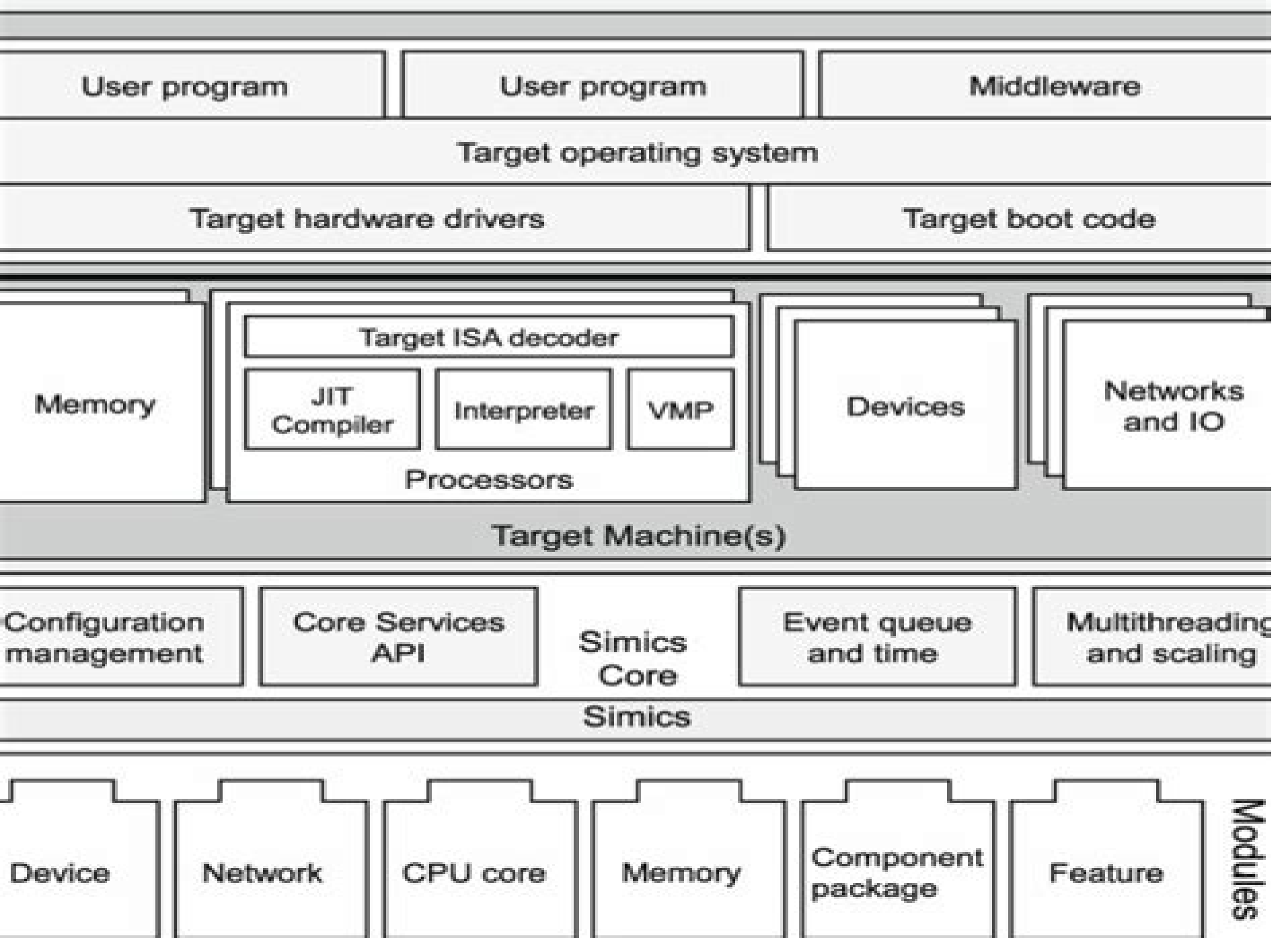




Processor And System On Chip Simulation

**Katalin Popovici, Frédéric
Rousseau, Ahmed A. Jerraya, Marilyn
Wolf**



Processor And System On Chip Simulation:

Processor and System-on-Chip Simulation Rainer Leupers, Olivier Temam, 2010-09-15 Simulation of computer architectures has made rapid progress recently The primary application areas are hardware software performance estimation and optimization as well as functional and timing verification Recent innovative technologies such as retargetable simulator generation dynamic binary translation or sampling simulation have enabled widespread use of processor and system on chip SoC simulation tools in the semiconductor and embedded system industries Simultaneously processor and SoC simulation is still a very active research area e g what amounts to higher simulation speed flexibility and accuracy speed trade offs This book presents and discusses the principle technologies and state of the art in high level hardware architecture simulation both at the processor and the system on chip level *Processor and System-on-Chip Simulation* Rainer Leupers, Olivier Temam, 2010 Processor and System on Chip Simulation Edited by Rainer Leupers Olivier Temam The current trend from monolithic processors to multicore and multiprocessor systems on chips MPSoC with tens of cores and gigascale integration makes hardware architecture and software design more and more complex and costly Therefore simulation technology has become an extremely important pre silicon verification and optimization vehicle Simulation of computer architectures has made rapid progress recently The primary application areas are hardware software performance estimation and optimization as well as functional and timing verification Recent innovative technologies such as retargetable simulator generation dynamic binary translation and sampling simulation have enabled widespread use of processor and system on chip SoC simulation tools in the semiconductor and embedded system industries This book presents and discusses the principle technologies and state of the art in high level architecture software simulation both at the processor and the system on chip level Presents state of the art and future trends in processor and SoC simulation Demonstrates how simulation helps to boost hardware and software design productivity Addresses simulation requirements and technologies in the multicore context Covers system aspects such as virtual platforms bus simulation caches power and design space exploration **Multi-Processor System-on-Chip 2**, 2021-03-31 A Multi Processor System on Chip MPSoC is the key component for complex applications These applications put huge pressure on memory communication devices and computing units This book presented in two volumes Architectures and Applications therefore celebrates the 20th anniversary of MPSoC an interdisciplinary forum that focuses on multi core and multi processor hardware and software systems It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world over the last two decades Multi Processor System on Chip 2 covers application specific MPSoC design including compilers and architecture exploration This second volume describes optimization methods tools to optimize and port specific applications on MPSoC architectures Details on compilation power consumption and wireless communication are also presented as well as examples of modeling frameworks and CAD tools Explanations of specific platforms for automotive and real time computing are also

included **Retargetable Processor System Integration into Multi-Processor System-on-Chip Platforms** Andreas Wieferink, Heinrich Meyr, Rainer Leupers, 2008-07-08 This book presents a methodology and the associated tooling for enabling design space exploration as well as a successive refinement flow for the design of optimized MP SoCs with a high degree of automation

Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms Tim Kogel, Rainer Leupers, Heinrich Meyr, 2006-08-25 We are presently observing a paradigm change in designing complex SoC as it occurs roughly every twelve years due to the exponentially increasing number of transistors on a chip This design discontinuity as all previous ones is characterized by a move to a higher level of abstraction This is required to cope with the rapidly increasing design costs While the present paradigm change shares the move to a higher level of abstraction with all previous ones there exists also a key difference For the first time shrinking geometries do not lead to a corresponding increase of performance In a recent talk Lisa Su of IBM pointed out that in 65nm technology only about 25% of performance increase can be attributed to scaling geometries while the lion share is due to innovative processor architecture 1 We believe that this fact will revolutionize the entire semiconductor industry What is the reason for the end of the traditional view of Moore's law It is instructive to look at the major drivers of the semiconductor industry wireless communications and multimedia Both areas are characterized by a rapidly increasing demand of computational power in order to process the sophisticated algorithms necessary to optimally utilize the precious resource bandwidth The computational power cannot be provided by traditional processor architectures and shared bus type of interconnects The simple reason for this fact is energy efficiency there exist orders of magnitude between the energy efficiency of an algorithm implemented as a hardware functionality computational element and of a software implementation on a processor

Embedded Software Design and Programming of Multiprocessor System-on-Chip Katalin Popovici, Frédéric Rousseau, Ahmed A. Jerraya, Marilyn Wolf, 2010-03-03 Current multimedia and telecom applications require complex heterogeneous multiprocessor system on chip MPSoC architectures with specific communication infrastructure in order to achieve the required performance Heterogeneous MPSoC includes different types of processing units DSP microcontroller ASIP and different communication schemes fast links non standard memory organization and access Programming an MPSoC requires the generation of efficient software running on MPSoC from a high level environment by using the characteristics of the architecture This task is known to be tedious and error prone because it requires a combination of high level programming environments with low level software design This book gives an overview of concepts related to embedded software design for MPSoC It details a full software design approach allowing systematic high level mapping of software applications on heterogeneous MPSoC This approach is based on gradual refinement of hardware software interfaces and simulation models allowing to validate the software at different abstraction levels This book combines Simulink for high level programming and SystemC for the low level software development This

approach is illustrated with multiple examples of application software and MPSoC architectures that can be used for deep understanding of software design for MPSoC *A System-level Platform-based Multi-core System-on-chip Simulation*

Framework with Retargetable Processing Element Models Jinwen Xi, 2007 **Applied Computational Intelligence in Engineering and Information Technology** Radu-Emil Precup, Szilveszter Kovács, Stefan Preitl, Emil M. Petriu, 2012-03-22

This book highlights the potential of getting benefits from various applications of computational intelligence techniques The present book is structured such that to include a set of selected and extended papers from the 6th IEEE International Symposium on Applied Computational Intelligence and Informatics SACI 2011 held in Timisoara Romania from 19 to 21 May 2011 After a serious paper review performed by the Technical Program Committee only 116 submissions were accepted leading to a paper acceptance ratio of 65 % A further refinement was made after the symposium based also on the assessment of the presentation quality Concluding this book includes the extended and revised versions of the very best papers of SACI 2011 and few invited papers authored by prominent specialists The readers will benefit from gaining knowledge of the computational intelligence and on what problems can be solved in several areas they will learn what kind of approaches is advised to use in order to solve these problems A very important benefit for the readers is an understanding of what the major difficulties are and the cost effective solutions to deal with them This book will offer a convenient entry for researchers and engineers who intend to work in the important fields of computational intelligence **Multiprocessor**

System-on-Chip Michael Hübner, Jürgen Becker, 2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx, Nadine Azemard, Philippe Maurine, 2006-09-07 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more

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