

Pre Public Examination
GCSE Mathematics (Edexcel style)
May 2017
Higher Tier
Paper 2H

Name

Class

TIME ALLOWED

1 hour 30 minutes

INSTRUCTIONS TO CANDIDATES

- Answer **all** the questions.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- **You are permitted to use a calculator in this paper.**
- Do all rough work in this book.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets () at the end of each question or part question on the Question Paper.
- **You are reminded of the need for clear presentation in your answers.**
- The total number of marks for this paper is **80**.

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Question	Mark	Out of
1		2
2		4
3		5
4		2
5		2
6		4
7		4
8		4
9		5
10		4
11		5
12		4
13		3
14		4
15		4
16		4
17		4
18		4
19		6
20		6
Total		80

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web as an alternative you can also write your simulation stimulus using generic vhdl code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libraries that are supported by almost all vhdl compilers specific silicon

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web for sample syntax and a list of vhdl statements supported by the vhdl synthesizer see appendix a quick reference for a list of exceptions and constraints on the vhdl synthesizer s support of vhdl see appendix b limitations this chapter shows you the structure of a vhdl design and then

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web from wikipedia the free encyclopedia vhdl source for a signed vhsic hardware description languagevhdl is a hardware description language hdl that can model the behavior and structure of at multiple levels of abstraction ranging from the system level down to that of logic gates for design entry documentation and verification purposes

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web feb 16 2023 by using the coding style above there is no question about which version of bottom is wanted the version in the library my lib1 is the correct one care should be taken when choosing library names for vhdl files while a library called work is a common library name for many projects the tool will handle it a little differently than

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web dec 29 2017 vhdl uses a similar description however it has its own syntax for example it uses the following lines of code to describe the input and output ports of this circuit 1 entity circuit 1 is 2 port a in std logic 3 b in std logic 4 out1 out std logic 5 end circuit 1

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web apr 29 2016 vhdl was created in the 1980s to develop a high speed integrated circuit it has since become an industry

standard language for describing digital systems at the structural or behavioral levels in a text based format the vhdl file can be used to manufacture a physical circuit such as a motherboard processor or memory module

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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web quartus and vhdl code in this section you should learn how to implement a vhdl code for single cycle data path before we go any further let s define some of the terms that we use throughout the book entity all designs are expressed in terms of entities an entity is the most basic building block in a design

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