CHAPTER

12

# **Designing Memory and Array Structures**

Memory classification and architecture

Data-storage cells for read-only, nonvolatile, and read-write memories

Peripheral circuits—sense amplifiers, decoders, drivers, and timing generators

Power consumption and reliability issues in memory design

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# **Rabaey Digital Integrated Circuits Chapter 12**

**Christian Piguet** 

#### **Rabaey Digital Integrated Circuits Chapter 12:**

The VLSI Handbook Wai-Kai Chen, 2018-10-03 For the new millenium Wai Kai Chen introduced a monumental reference for the design analysis and prediction of VLSI circuits The VLSI Handbook Still a valuable tool for dealing with the most dynamic field in engineering this second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts models and equations Written by a stellar international panel of expert contributors this handbook is a reliable comprehensive resource for real answers to practical problems It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus WHAT S IN THE SECOND EDITION Sections on Low power electronics and design VLSI signal processing Chapters on CMOS fabrication Content addressable memory Compound semiconductor RF circuits High speed circuit design principles SiGe HBT technology Bipolar junction transistor amplifiers Performance modeling and analysis using SystemC Design languages expanded from two chapters to twelve Testing of digital systems Structured for convenient navigation and loaded with practical solutions The VLSI Handbook Second Edition remains the first choice for answers to the problems and challenges faced daily in engineering practice **VLSI Systems** Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental Low-Voltage/Low-Power Integrated Circuits and Systems Edgar Sánchez-Sinencio, Andreas G. understanding Andreou, 1999-01-13 Electrical Engineering Low Voltage Low Power Integrated Circuits and Systems Low Voltage Mixed Signal Circuits Leading experts in the field present this collection of original contributions as a practical approach to low power analog and digital circuit theory and design illustrated with important applications and examples Low Voltage Low Power Integrated Circuits and Systems features comprehensive coverage of the latest techniques for the design modeling and characterization of low power analog and digital circuits Low Voltage Low Power Integrated Circuits and Systems will help you improve your understanding of the trade offs between analog and digital circuits and systems It is an invaluable resource for enhancing your designs This book is intended for senior and graduate students It is also intended as a key reference for designers in the semiconductor and communication industries Highlighted applications include Low voltage analog filters Low power multiplierless YUV to RGB based on human vision perception Micropower systems for implantable defibrillators and pacemakers Neuromorphic systems Low power design in telecom circuits **Negative Capacitance** Field Effect Transistors Young Suh Song, Shubham Tayal, Shiromani Balmukund Rahi, Abhishek Kumar Upadhvav, 2023-10-31 This book aims to provide information in the ever growing field of low power electronic devices and their applications in portable devices wireless communication sensor and circuit domains Negative Capacitance Field Effect Transistors Physics Design Modeling and Applications discusses low power semiconductor technology and addresses state of

the art techniques such as negative capacitance field effect transistors and tunnel field effect transistors. The book is split into three parts The first part discusses the foundations of low power electronics including the challenges and demands and concepts such as subthreshold swing The second part discusses the basic operations of negative capacitance field effect transistors NCFETs and tunnel field effect transistors TFETs The third part covers industrial applications including cryogenics and biosensors with NC FET This book is designed to be a one stop guide for students and academic researchers to understand recent trends in the IT industry and semiconductor industry It will also be of interest to researchers in the field of nanodevices such as NC FET FinFET tunnel FET and device circuit codesign Thermal and Power Management of Integrated Circuits Arman Vassighi, Manoj Sachdev, 2006-06-01 In Thermal and Power Management of Integrated Circuits power and thermal management issues in integrated circuits during normal operating conditions and stress operating conditions are addressed Thermal management in VLSI circuits is becoming an integral part of the design test and manufacturing Proper thermal management is the key to achieve high performance quality and reliability Performance and reliability of integrated circuits are strong functions of the junction temperature A small increase in junction temperature may result in significant reduction in the device lifetime This book reviews the significance of the junction temperature as a reliability measure under nominal and burn in conditions The latest research in the area of electro thermal modeling of integrated circuits will also be presented Recent models and associated CAD tools are covered and various techniques at the circuit and system levels are reviewed Subsequently the authors provide an insight into the concept of thermal runaway and how it may best be avoided A section on low temperature operation of integrated circuits concludes the book **Electronics Design** Christian Piquet, 2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices. The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today s methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now **Low-Power CMOS Circuits** Christian Piquet, 2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet's recently published Low Power

Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools addresses the design of low power circuitry in deep submicron technologies It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers Providing detailed examinations contributed by leading experts Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems Minimizing and Exploiting Leakage in VLSI Design Nikhil Jayakumar, Suganth Paul, Rajesh Garg, 2009-12-02 Power consumption of VLSI Very Large Scale Integrated circuits has been growing at an alarmingly rapid rate This increase in power consumption coupled with the increasing demand for portable hand held electronics has made power consumption a dominant concern in the design of VLSI circuits today Traditionally dynamic switching power has dominated the total power consumption of an IC However due to current scaling trends leakage power has now become a major component of the total power consumption in VLSI circuits Leakage power reduction is especially important in portable hand held electronics such as cell phones and PDAs This book presents two techniques aimed at reducing leakage power in digital VLSI ICs The first technique reduces leakage through the selective use of high threshold voltage sleep transistors The second technique reduces leakage by applying the optimal Reverse Body Bias RBB voltage This book also shows readers how to turn the leakage problem into an opportunity through the use of sub threshold logic

Closing the Gap Between ASIC & Custom David Chinnery, Kurt William Keutzer, 2002 This book carefully details design tools and techniques for high performance ASIC design Using these techniques the performance of ASIC designs can be improved by two to three times Important topics include Improving performance through microarchitecture Timing driven floorplanning Controlling and exploiting clock skew High performance latch based design in an ASIC methodology Automatically identifying and synthesizing complex logic gates Automated cell sizing to increase performance and reduce power Controlling process variation These techniques are illustrated by designs running two to three times the speed of typical ASICs in the same process generation Micro-Relay Technology for Energy-Efficient Integrated Circuits Hei Kam, Fred Chen, 2014-10-16 This volume describes the design of relay based circuit systems from device fabrication to circuit micro architectures This book is ideal for both device engineers as well as circuit system designers and highlights the

importance of co design across design hierarchies when trying to optimize system performance in this case energy efficiency The book will also appeal to researchers and engineers focused on semiconductor integrated circuits and energy efficient electronics Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise **Design Essentials** Jan Rabaey, 2009-04-21 Low Power Design Essentials contains all the topics of importance to the low power designer The book lays the foundation with background chapters entitled Advanced MOS Transistors and Their Models and Power Basics These chapters are followed by chapters on the design process including optimization architecture and algorithm level memory run time standby logic and standby memory Chapters on special topics are also included power management and modal design ultra low power and low power design methodology and flows The book concludes with a chapter on case studies as well as a chapter on Projection into the Future These chapters are all based on the extensive amount of teaching that the author has carried out both at universities and companies worldwide All chapters have been drawn up specifically for self study They aim however at different levels of understanding All the chapters start with elementary material but most also contain advanced material Smart and Intelligent Systems Subhojit Dawn, Kedar Nath Das, Rammohan Mallipeddi, Debi Prasanna Acharjya, 2021-08-30 This book is a collection of high quality research papers presented at the International Conference on Smart and Intelligent Systems SIS 2021 which will be held in Velagapudi Ramakrishna Siddhartha Engineering College VRSEC Andhra Pradesh India during February 25 26 2021 in virtual mode It highlights how recent informatics intelligent systems have successfully been used to develop innovative smart techniques and infrastructure in the field of modern engineering and technology. The book will also be of interest to those working in the field of computational intelligence smart computer network and security analysis control and automation system cloud computing fog computing and IoT smart grid communication smart cities solar cell synthesis and their performance green technology and many more The contents of this book prove useful to researchers and professionals Nanometer CMOS ICs Harry Veendrick, 2024-10-21 This textbook provides a comprehensive fully updated introduction to the essentials of nanometer CMOS integrated circuits It includes aspects of scaling to even beyond 3nm CMOS technologies and designs It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design fabrication and application Coverage includes all associated disciplines of nanometer CMOS ICs including physics lithography technology design memories VLSI power consumption variability reliability and signal integrity testing yield failure analysis packaging scaling trends and road blocks The text is based upon in house Philips NXP Semiconductors

Applied Materials ASML IMEC ST Ericsson Infineon TSMC etc courseware which to date has been completed by more than 7000 engineers working in a large variety of the above mentioned disciplines Fast Hopping Frequency Generation in Digital CMOS Mohammad Farazian, Lawrence E. Larson, Prasad S. Gudem, 2012-10-12 Overcoming the agility limitations of conventional frequency synthesizers in multi band OFDM ultra wideband is a key research goal in digital technology This volume outlines a frequency plan that can generate all the required frequencies from a single fixed frequency able to implement center frequencies with no more than two levels of SSB mixing It recognizes the need for future synthesizers to bypass on chip inductors and operate at low voltages to enable the increased integration and efficiency of networked appliances The author examines in depth the architecture of the dividers that generate the necessary frequencies from a single base frequency and are capable of establishing a fractional division ratio Presenting the first CMOS inductorless single PLL 14 band frequency synthesizer for MB OFDMUWB makes this volume a key addition to the literature and with the synthesizer capable of arbitrary band hopping in less than two nanoseconds it operates well within the desired range on a 1 2 volt power supply The author's close analysis of the operation stability and phase noise of injection locked regenerative frequency dividers will provide researchers and technicians with much food for developmental thought Circuits and Systems for Future Generations of Wireless Communications Aleksandar Tasic, Wouter A. Serdijn, Gianluca Setti, 2009-05-16 The idea for this book originated from a Special Session on Circuits and Systems for Future Generations of Wireless Communications that was presented at the 2005 International Symposium on Circuits and Systems which was then followed by two Special Issues bearing the same title that appeared in the March and April 2008 issues of the IEEE Transactions on Circuits and Systems Part II Express Briefs Out of a large number of great contributions we have selected those tting best the book format based on their quality We would like to thank all the authors the reviewers of the Transactions on Circuits and Systems Part II and the reviewers of the nal book material for their efforts in creating this manuscript We also thank the Springer Editorial Staff for their support in putting together all the good work We hope that this book will provide you the reader with new insights into Circuits and Systems for Future Generations of Wireless Communications Architectures for Baseband Signal Processing Frank Kienle, 2013-08-15 This book addresses challenges faced by both the algorithm designer and the chip designer who need to deal with the ongoing increase of algorithmic complexity and required data throughput for today s mobile applications. The focus is on implementation aspects and implementation constraints of individual components that are needed in transceivers for current standards such as UMTS LTE WiMAX and DVB S2 The application domain is the so called outer receiver which comprises the channel coding interleaving stages modulator and multiple antenna transmission Throughout the book the focus is on advanced algorithms that are actually in use in modern communications systems Their basic principles are always derived with a focus on the resulting communications and implementation performance As a result this book serves as a valuable reference for two

typically disparate audiences in communication systems and hardware design Dual Mode Logic Itamar Levi, Alexander Fish,2020-12-15 This book presents Dual Mode Logic DML a new design paradigm for digital integrated circuits DML logic gates can operate in two modes each optimized for a different metric Its on the fly switching between these operational modes at the gate block and system levels provide maximal E D optimization flexibility Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability All the facets of the DML methodology are covered starting from basic concepts through single gate optimization general module optimization design trade offs and new ways DML can be integrated into standard design flows using standard EDA tools DML logic is compatible with numerous applications but is particularly advantageous for ultra low power reliable high performance systems and advanced scaled technologies Written in language accessible to students and design engineers each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic Describes a novel promising alternative to conventional CMOS logic known as Dual Mode Logic DML with which a single gate can be operated selectively in two modes each optimized for a different metric e q energy consumption performance size Demonstrates several techniques at the architectural level which can result in high energy savings and improved system performance Focuses on the tradeoffs between power area and speed including optimizations at the transistor and gate level including alternatives to DML basic cells Illustrates DML efficiency for a variety of VLSI applications **Interconnect Technologies for** Integrated Circuits and Flexible Electronics Yash Agrawal, Kavicharan Mummaneni, P. Uma Sathyakam, 2023-09-21 This contributed book provides a thorough understanding of the basics along with detailed state of the art emerging interconnect technologies for integrated circuit design and flexible electronics It focuses on the investigation of advanced on chip interconnects which match the current as well as future technology requirements. The contents focus on different aspects of interconnects such as material physical characteristics parasitic extraction design structure modeling machine learning and neural network based models for interconnects signaling schemes varying signal integrity performance analysis variability reliability aspects associated electronic design automation tools The book also explores interconnect technologies for flexible electronic systems It also highlights the integration of sensors with stretchable interconnects to demonstrate the concept of a stretchable sensing network for wearable and flexible applications. This book is a useful guide for those working in academia and industry to understand the fundamentals and application of interconnect technologies **Energy Efficient** Microprocessor Design Thomas D. Burd, Robert W. Brodersen, 2012-12-06 This work began in 1995 as an outgrowth of the InfoPad project which showed us that in order to reduce the energy consumption of a portable multimedia terminal that something had to be done about the consumption of the microprocessor subsystem. The design of the InfoPad attempted to reduce the requirements of this general pur pose processor by moving the computation into the network or by the use of

highly optimized integrated circuits but in spite of these efforts it still was a major consumer of energy The reasons for this became apparent as we determined that the energy required to perform a function in dedicated hardware could be several orders of magnitude lower than that consumed in the InfoPad microprocessor We therefore set out on a full fledged attack on all aspects of the microprocessor energy consumption 1 J After considerable analysis it became clear that though better circuit design and a stream lined architecture would assist in our goal of energy reduction that the biggest gains were to be found by operating at reduced voltages For the busses and VO this could be accomplished without significant degradation of the processor performance but this was not a straightforward solution when applied to the core of the processor sub system CPU and memory

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