

CourseCode-21EE32

Model Question Paper (CBCS Scheme)

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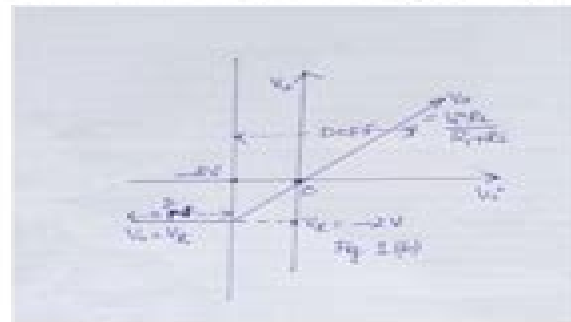
Third Semester BE Degree Examination Course Title– Analog Electronic Circuits and Op amps

TIME: 03 Hours

Max.Marks:100

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

Q.No.	Module1		Marks
Q1	a	Explain the static resistance and dynamic resistance of a diode.	06
	b	Design a shunt clipping circuit for the transfer characteristic as shown in Fig.1 (b). Assume that a resistance of $1K\Omega$ is connected in series with input sinusoidal signal and output is taken across $RL = 10K\Omega$. Draw the input and output voltage waveforms.	07
	c	Define stability factor and derive an expression for stability factor S in a voltage divider bias circuit.	08
OR			
Q2	a	For the transistor amplifier in general form obtain expressions for current gain, input resistance, voltage gain and output resistance using h-parameter model	10
	b	Draw and explain the negative clamper circuit. Sketch the input and voltage waveforms.	05
	c	For the emitter follower configuration, derive expressions for current gain and input resistance using simplified hybrid model.	05
Module 2			
Q3	a	For the Darlington connection , explain the analysis of second and first stage in terms of current gain and input resistance . Use h-parameter model.	12
	b	Explain the concept of feedback with suitable block diagrams.	08
OR			



Sample Question Paper Third Semester G Scheme

Robert T. Grauer



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